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ADVANCED SEMICONDUCTOR PACKAGING MATERIALS FOR WAFER LEVEL AND 2.5/3D APPLICATIONS

RUUD DE WIT | HENKEL ELECTRONIC MATERIALS
NIJMEGEN | 6-7 SEPTEMBER 2023

European Packaging, Assembly and Test | Workshop 2023

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OUR PLAYGOUND AND FIELDS OF EXPERTISE

Improving the electronics technologies of today, for the advances of tomorrow

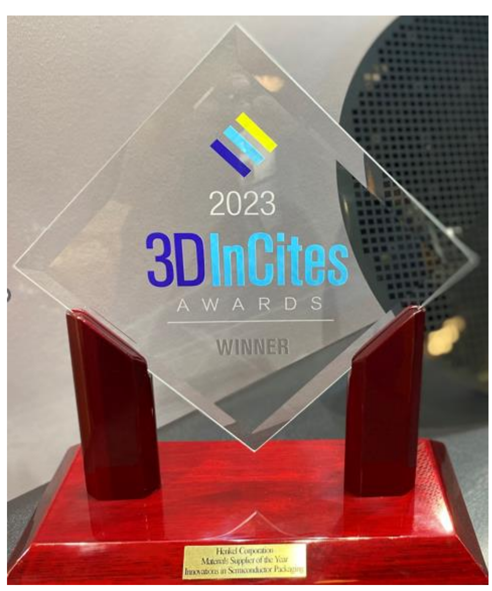
BOARD, MODULE AND COMPONENT ASSEMBLY MATERIALS FOR CONSUMER ELECTRONICS

MATERIALS FOR SEMICONDUCTOR BACK-END ASSEMBLY

Consumer Devices **Modules & Components** **Semiconductor Packaging**

OUR PLAYGOUND AND FIELDS OF EXPERTISE

Henkel's 'Innovations in Semiconductor Packaging' have been recognized and rewarded with the 3DInCites 'Materials Supplier of the Year' Award

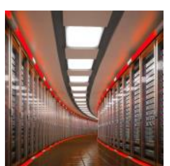


3D InCites Editorial Director Françoise von Trapp said, *"Developing solutions for the most pressing materials challenges for today's semiconductor packaging technologies is no easy feat. To tackle several in one year demonstrates Henkel's commitment to the future heterogenous integration. Congratulations on winning this award – it's well deserved."*

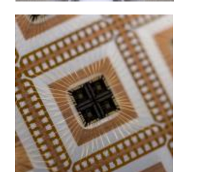
3D InCites is an online information resource focused on semiconductor advanced packaging and heterogeneous integration. This year's 3D InCites Awards program included 36 nominees across 10 categories, with a panel of 4 judges and results from online voting determining the winners.

OUR SEMICONDUCTOR FOCUS MARKETS AND PACKAGING MATERIAL SOLUTIONS

- 5G/Telecom/ Mobile
- Data Center/ Memory



- Automotive/ Industrial



Liquid Compression Molding (LCM)

EMI Shielding Materials (Trench Fill & Coatings)

Wafer Back Side Protection (BSP)

Non-Conductive FILM (NCF)

Non-Conductive PASTE (NCP), Capillary Underfill (CUF)

Liquid Encapsulation (Dam & Fill, Glob Top)

Die Attach PASTE (incl. Silver Sintering)

Die Attach FILM

Electrically Conductive Adhesives (ECA)

CONTENT

- Challenges in Advanced Flip Chip and Heterogeneous Integration
- Enabling Semi Packaging Material Solutions
  - Liquid Wafer Level Encapsulation (LCM, MUF, LDS)
  - Advanced Capillary Underfills (post-applied)
- Key Takeaways

SEMICONDUCTOR PACKAGING

MARKET SEGMENTS AND TRENDS

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5G / Telecom / Mobile

- **Increased integration** for **RF front-end** and **application processor** (AP)
- **Higher frequency**, wide band gap IC's
- **Higher power**, more heat dissipation
- **Higher reliability**

Data center / Memory

- **Heterogeneous integration**, chiplet style packaging and 3D integration
- **Larger chip** and **larger body** architectures
- **Lower power** and **higher I/O** densities for high performance computing (HPC)

Automotive / Industrial

- **Increasing sensor and IC content** for sensing & signal conditioning
- **Data processing**, zonal or domain architectures with large body FC-BGA's
- **More power electronics for (H)EV**, higher density and efficiency (SiC, GaN)

PACKAGING CHALLENGES

SERVER AND CLIENT PROCESSOR APPLICATIONS

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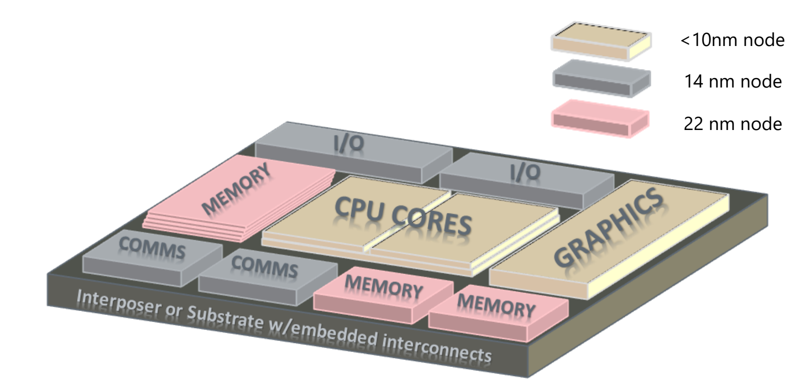
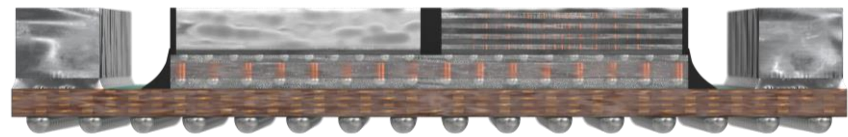
- **Warpage** – Stress and co-planarity issues arising due to large body packages (>80 x 80mm)
- **Processing** – Challenges in flow behavior and process time for large die, high I/O, handling and warpage issues in WLP process, challenges in process and materials for 2.5D/3D stacking, etc.
- **Integration** – Die level, package level and WLP integration issues due to complexity of new package architectures, (incl. chiplets), pitch and gap scaling of back-end I/O
- **Thermal** – Higher thermal loading and dissipation requirements, impact on design and performance
- **Reliability** – Expanding reliability requirements incl. automotive grade conditions for advanced flip chip processors



Schematic view of CHIPLET integration found in HPC server



Schematic X-section of 2.5D integrated package for processors & accelerators

PACKAGING CHALLENGES

MOBILE PROCESSOR APPLICATIONS

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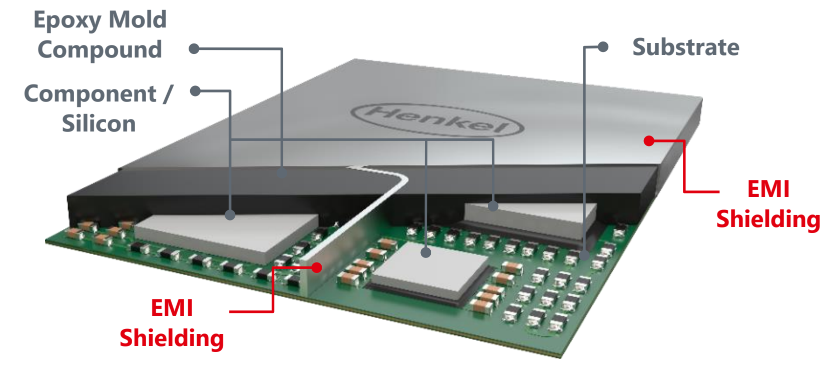
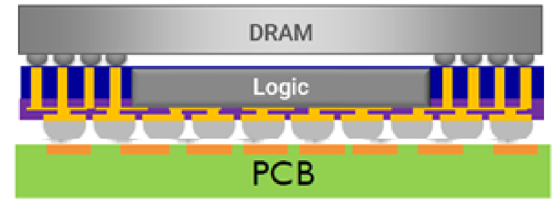
- **Processing** – Challenges in packaging architectures for high end mobile applications processors and RF front-end covering flip chip, embedding, PoP, SiP and new evolving architectures
- **EMI Shielding** – Complex shielding requirements for RF front end and memory devices involving conformal and compartmental shielding
- **Integration** – Complex architectures involving multi-die, multi-component integration in RF front-end, die stacking, package stack integrations in mobile application processors
- **Thermal** – Higher thermal density from WBG devices in RF power amplifiers, increasing thermal requirements from advanced mobile processors



Schematic example of System-in-Package (SiP) in RF Front End



Schematic X-section of Fan-Out Package-on-Package (FO-PoP) for mobile application processors

SEMICONDUCTOR PACKAGING
ENABLING MATERIAL SOLUTIONS

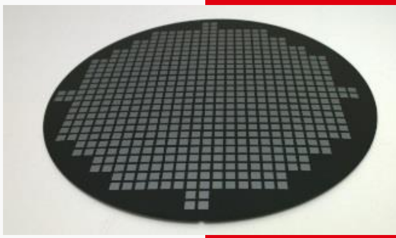
Semiconductor Packaging Materials

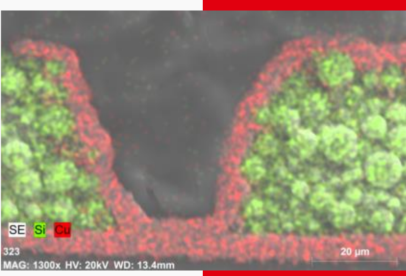
- **WIREBOND Packaging**
  - **Die Attach PASTE**
    - Conductive (Ag filled)
      - Medium (<20 W/mK)
      - High (20-50 W/mK)
      - Sintering (>50 W/mK)
    - Non-Conductive
  - **Die Attach FILM**
    - Conductive (Ag filled)
    - Non-Conductive
  - **Pre-Applied Die Attach**
    - Conductive (Ag filled)
    - Non-Conductive
    - Print Board-on-Chip
  - **Encapsulants**
    - Cavity / Side Fill
    - Dam & Fill
    - Glob Top
- **ADVANCED Packaging**
  - **Underfills**
    - Capillary (post-applied)
    - Non-Cond. Paste *)
    - Non-Cond. Film *)
  - **Wafer Level Encapsulation**
    - Liquid Compression
    - Stencil Printable
    - Backside Protection
  - **Lid / Stiffener Attach**
    - Conductive (Ag filled)
    - Non-Conductive
  - **EMI Shielding**
    - Compartment (trench fill)
    - Conformal (coating)

*) Pre-Applied Underfill for Thermal Compression Bonding

CONTENT

- Challenges in Advanced Flip Chip and Heterogeneous Integration
- Enabling Semi Packaging Material Solutions
  - **Liquid Wafer Level Encapsulation (LCM, MUF, LDS)**
  - Advanced Capillary Underfills (post-applied)
- Key Takeaways



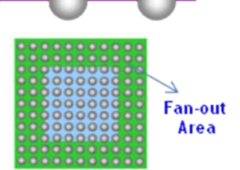


LIQUID WAFER LEVEL ENCAPSULATION

TARGET APPLICATIONS

Fan Out Wafer Level Packaging (FOWLP)

- Liquid Compression Molding (LCM)

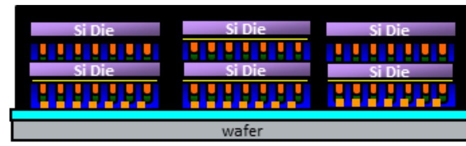


Fan In Wafer Level Packaging (WLCSP)

- 5 or 6 Side Si Chip Protection
- Molding or Printing Process

Chip on Wafer (CoW) / 2.5D/3D Heterogeneous Integration

- Overmolding Process (LCM)
- Gap Filling LCM or **Molded Underfill (MUF)**



LIQUID WAFER LEVEL ENCAPSULATION

PRODUCT DEVELOPMENT FOCUS

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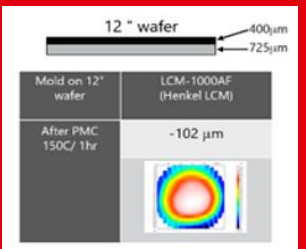
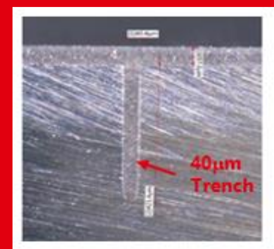
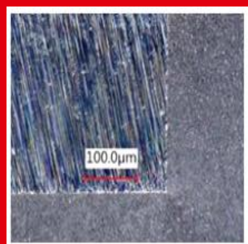
Sustainability	Ultra-low warpage	Small gap filling	Robust reliability
			
▪ Anhydride free epoxy resin base chemistry ▪ REACH compliant - SVHC free - PFAS free	▪ Ultra-low warpage on Wafer and Panel Level ▪ Low warpage stability during post processing (RDL, PI application)	▪ Ultra-fine Si fillers from 10um down to 1.5um filler cut while maintaining good flow ▪ Enabling trench filling for 5/6 side WLCSP protection and underfilling down to 10-40um gap depending on design	▪ High Tg (>140°C) and low CTE to limit thermal expansion differences ▪ Passing MSL1 and >1000 TC (-55C to 125°C) on specific packages

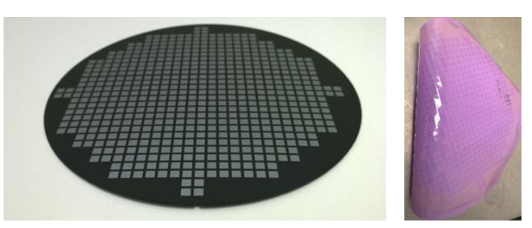
LIQUID WAFER LEVEL ENCAPSULATION
PRODUCT PORTFOLIO EVOLUTION

LCM 1000AF	LCM 1000AG-1	EN 8000AJ	LCM-MUF-1	LCM-MUF-2/3
▪ **Launched for FI-/ FO-WLP market** ▪ REACH compliant base chemistry (anhydride free) ▪ Proven process on Towa and Yamada molding equipment with Mitsui TR tape ▪ Good reliability	▪ **Low warpage over-mold for 2.5D WLP** ▪ High adhesion to Si and SiN in HBM ▪ Improved strength and strain for crack resistance during temp cycling ▪ Good reliability	▪ **Low warpage, stencil printable WLP encapsulant** - Stencil or screen - Vacuum capable ▪ Lower modulus ▪ PI compatible ▪ MSL1 on WLCSP ▪ Good reliability	▪ **Overmolding and underfilling 2.5D/3D packages** ▪ Void-free gap fill down to 25um ▪ Low viscosity and IMC temp (120°C) ▪ CMP compatible ▪ Passing all reliability requirements	▪ **Overmolding and underfilling HBM packages** ▪ **Void-free gap fill down to 10um** ▪ Low viscosity and IMC temp (120°C) ▪ High filler loading with <3um cut ▪ High toughness

LIQUID WAFER LEVEL ENCAPSULATION

OVERMOLDING (COMPRESSION OR *PRINTING*)

- **Low warpage** after PMC, RDL process simulation (220°C) and 24h relaxation



IMC=120°C/5min PMC=150°C/1hr	LOCTITE® ECCOBOND LCM 1000AF
Prebake at 130°C, de-tape at 100°C	MITSUI ICROS® RT-A4098-2 Thermal Release Tape
Warpage after PMC (12"x 500um FO)	**0.39mm**
Warpage after 220°C/1hr	**0.92mm**
Warpage after 220°C/2hrs	**1.31mm**

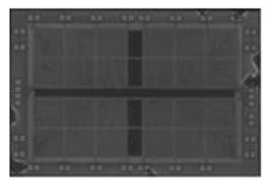
Product Name	**LCM 1000AF**	**LCM 1000-AG1**	***EN 8000AJ***
Product status	Commercial	Development	*Scale up*
Target applications	FOWLP, WLCSP	CoW, 2.5D	*WLCSP*
Filler cut (um)	**10**	**10**	***10***
Viscosity (25°C, Pa·s)	**~800**	**~800**	***~60***
Tg by TMA (°C)	**~160**	**~140**	***~145***
CTE1 / CTE2 (ppm/(°C)	**7 / 18**	**6 / 16**	***12 / 28***
Modulus @ 25°C (GPa)	**~15**	**~15**	***10***
In mold cure / *Staging*	5min @ 120°C	5min @ 120°C	*1hr @ 70°C*
Post mold cure (PMC)	1hr @ 150°C	1hr @ 150°C	*1hr @ 150°C*
Key features	Low warpage after RDL, PI	Low warpage, high toughness	*Low viscosity for printing*
Suitable for			Chip

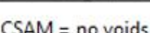
LIQUID WAFER LEVEL ENCAPSULATION

MOLDED UNDERFILL (LCM-MUF)

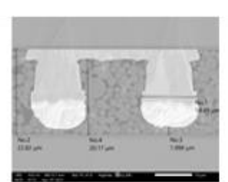
- Developed for **overmolding and underfilling** Chip-on-Wafer, 3D and High Bandwidth Memory packages in **1-step** with void-free gap-filling

- LCM MUF-1 successfully evaluated in HBM2 test vehicles (20um gap height, 36um bump pitch, 27K bump count, 7x11mm die size)





CSAM = no voids



SEM xsection = no voids

Product Name	LCM-MUF-1	LCM-MUF-2	LCM-MUF-3
Product status	Development	Development	Development
Target applications	2.5D, 3D	HBM	HBM
Filler cut (um)	**5**	**3**	**1.5**
Viscosity (25°C, Pa·s)	~170	~40	~50
Tg by TMA (°C)	~115	~135	~125
CTE1 / CTE2 (ppm/(°C)	9 / 24	15 / 31	16 / 33
Modulus @ 25°C (GPa)	13	10	10
In mold cure (IMC)	5min @ 120°C	5min @ 120°C	5min @ 120°C
Post mold cure (PMC)	1hr @ 150°C	1hr @ 150°C	1hr @ 150°C
Key features	Low warpage, gap fill <25um	Low warpage, gap fill <15um	Low warpage, gap fill <10um
Suitable for			

LIQUID WAFER LEVEL ENCAPSULATION

LASER DIRECT STRUCTURING AND CU PLATING (LDS)

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- LPKF's Active Mold Packaging (AMP) combines Laser Direct Structuring (LDS) technology with Epoxy Mold Compounds (EMC) for **electrical circuitry integration** directly **inside and onto molded package**

Flip Chip RDL
Antenna-on/in-Package
Package-on-Package
Conformal & Compartment Shielding
Stacked VIAs
IPD
SMD
Plugged/ Filled Via
Thermal Vias & Heat Sink

Courtesy of
LPKF
Laser & Electronics

LIQUID WAFER LEVEL ENCAPSULATION

LASER DIRECT STRUCTURING AND CU PLATING (LDS)

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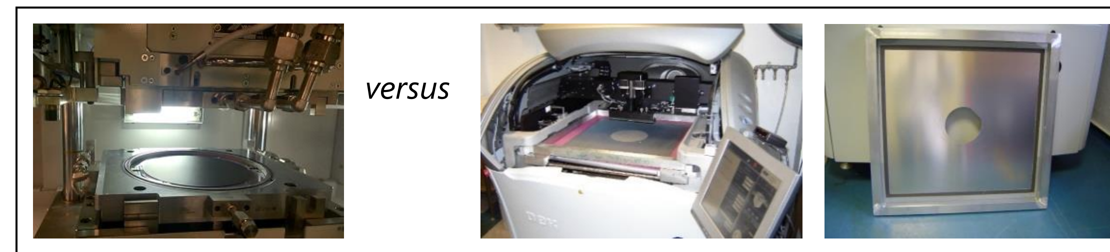
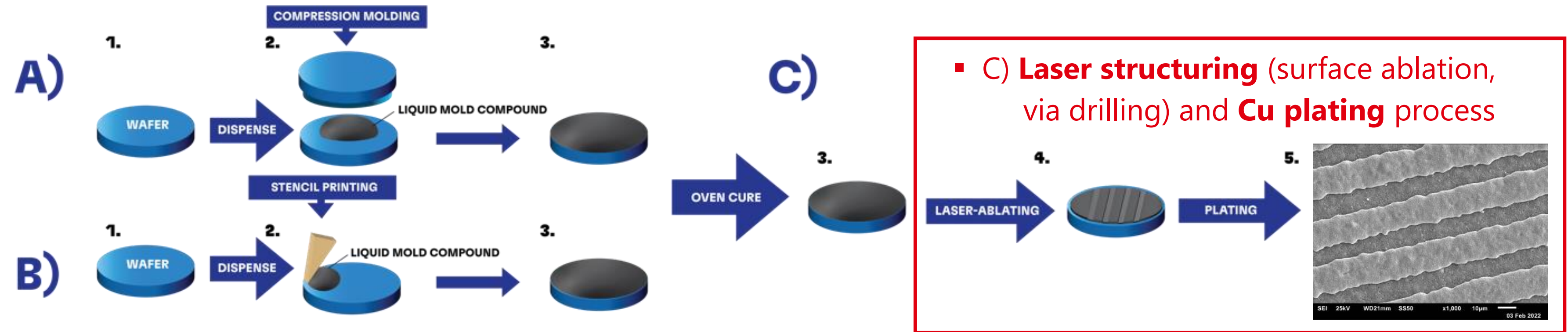
- A) **Liquid Compression Molding (LCM)**

  versus

- B) **Stencil Printing** encapsulation process





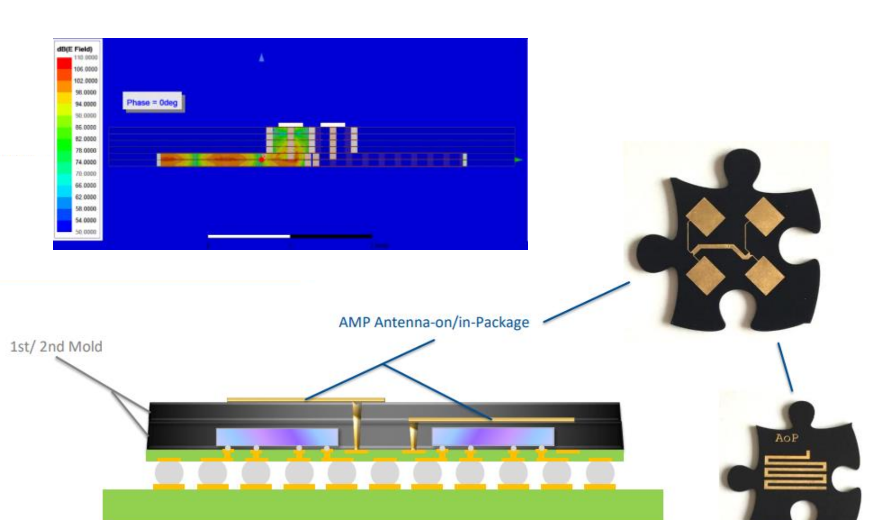
- C) **Laser structuring** (surface ablation, via drilling) and **Cu plating** process

LIQUID WAFER LEVEL ENCAPSULATION

5 IDENTIFIED 'LIQUID AMP' APPLICATIONS (LDS)

Courtesy of

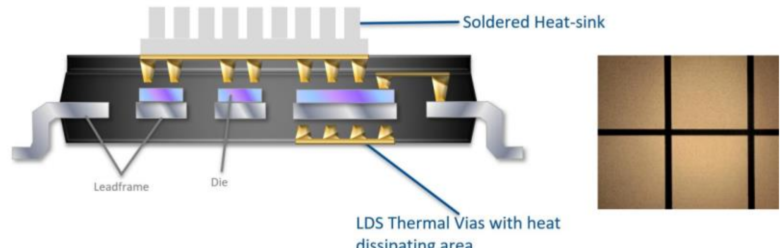
- **5G mmWave & 6G Antenna-on/in-Package**



- **(Selective) Conformal/Compartment EMI Shielding**

Conformal EMI Shielding
Compartment EMI Shielding
1st/ 2nd Mold
EMI

- **Heat Dissipation from Embedded Dies using "Thermal Vias" and "Heat Pads"**



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LIQUID WAFER LEVEL ENCAPSULATION

5 IDENTIFIED 'LIQUID AMP' APPLICATIONS (LDS)

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Courtesy of

- **Solderable SMD Component Terminations using Wafer Level 5/6 Side Protection**
- **Wire Bond Replacement by "Flat Bonds"**

OLD
Conventional Wire Bond package
traditional wire bond

AMP
Bond-less/ Flat-Bond package
Flat Bond Interconnect

LIQUID WAFER LEVEL ENCAPSULATION

HENKEL LDS DEVELOPMENT STATUS

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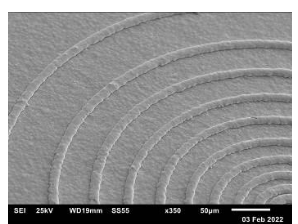
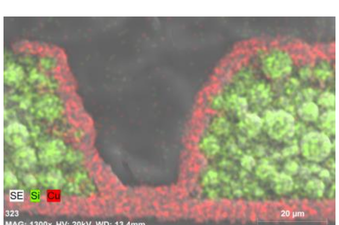
- Based on Henkel internal test data and LPKF's LDS and Cu plating test feedback, Henkel is offering 2 LDS formulations LOCTITE® ECCOBOND **LCM 1070LS** and **EN 8070LS** for sampling and feasibility investigation to customers for potential applications
- Further investigation towards **thinner layers and vias <50um and ~10/10um L/S** using smaller fillers
  - 20/20um and 15/15um L/S and ~30-40um plated vias have been demonstrated



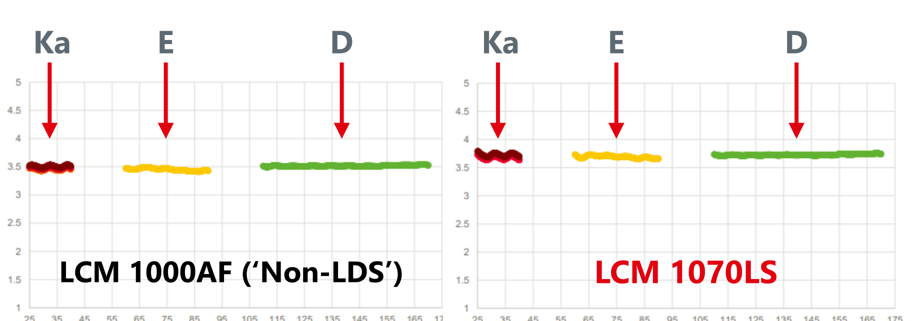


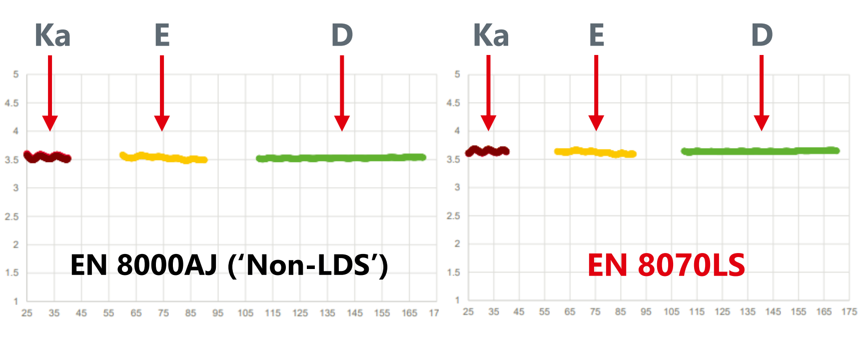
LOCTITE® ECCOBOND	LCM 1070LS	EN 8070LS
Application Process	**Compression Molding**	**Stencil Printing**
Production status	Development	
Filler content level	High	Medium
Density (g/cc)	>2	>2
Viscosity @ 25°C (Pa.s)	**~500**	**~70**
Tg by TMA (°C)	**158**	**144**
CTE1/CTE2 (ppm/°C)	**9/19**	**12/33**
Modulus @ 25°C (GPa)	**18**	**10**
In-Mold Cure (IMC) + Post Mold Cure (PMC)	120°C/5min + 150°C/1hr	70°C/60min + 150°C/1hr

LIQUID WAFER LEVEL ENCAPSULATION

HIGH FREQUENCY DIELECTRIC PROPERTIES UP TO 170 GHZ

- **3.5-3.7 Dielectric Constant (Dk)** over **25-170 GHz range** for all encapsulants measured on MCK equipment (https://mck.swissto12.ch)
  - No significant difference in dielectric performance between
    - **25-40 GHz** (Ka band), **60-90 GHz** (E band) and **110-170 GHz** (D band)
    - Highly filled molding and medium filled printing versions
    - Formulations with and without LDS additive





LIQUID WAFER LEVEL ENCAPSULATION

NEAR INFRA RED BLOCKING OF THIN EN 8070LS LAYERS

- 30-100um thin layers of EN 8070LS printed on glass using PI tapes as stencil (cured 1hr 70°C, 3hrs 150°C)
- Spectra recorded with Bruker MPA TM FT-NIR spectrometer (with blank glass slide analyzed as transmission background)
- EN 8070LS layers were measured same way at 3 positions with **NIR transmittance values of ~0.01% @ 1220nm for ~40um layer thickness** (~8200 cm-1 Wavenumber)

Wavelength [nm] Wavenumber [cm-1]	1180 8474	1200 8332	**1220 8197**	1300 7691	1400 7144
EN 8070LS **33UM**	0,00%	0,04%	**0,05%**	0,06%	0,11%
EN 8070LS **41UM**	0,00%	0,01%	**0,01%**	0,01%	0,03%
EN 8070LS **87UM**	0,00%	0,00%	**0,00%**	0,00%	0,00%
EN 8070LS **97UM**	0,00%	0,00%	**0,00%**	0,00%	0,00%

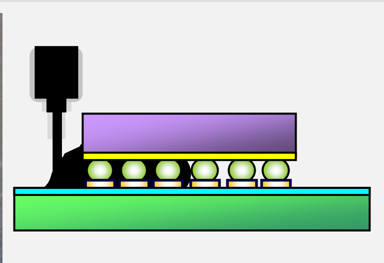
CONTENT

- Challenges in Advanced Flip Chip and Heterogeneous Integration
- Enabling Semi Packaging Material Solutions
  - Liquid Wafer Level Encapsulation (LCM, MUF, LDS)
  - **Advanced Capillary Underfills (post-applied)**
- Key Takeaways

ADVANCED UNDERFILL SOLUTIONS

POST-APPLIED VS PRE-APPLIED

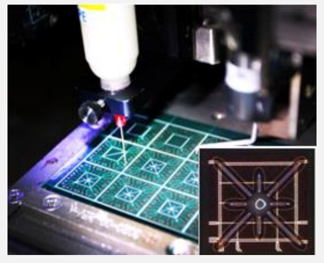
CAPILLARY UNDERFILL (CUF)



+ **Dominant technology**
+ **High UPH**

- ***No bump protection after chip attach***

NON-CONDUCTIVE PASTE (NCP)



+ **Enable fine pitch, narrow gap**
+ **Tight design by fillet control**
+ **Bump protection after bonding**

- ***Lower UPH vs CUF***

NON-CONDUCTIVE FILM (NCF)

+ **Enable fine pitch, narrow gap**
+ **Tight design by fillet control**
+ **Thin wafer processing**

- ***Different film thickness depending on bump height***

Post-Applied | **Pre-Applied**

CAPILLARY UNDERFILL BASICS

FULL VERSUS PARTIAL UNDERFILLS

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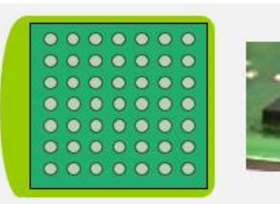
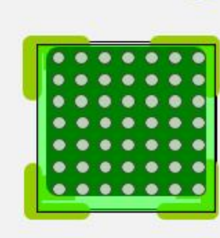
- **Full Capillary Underfill**
  - Dispensed after reflow along edge(s) with “L” or “I” shape
  - Flows under component and fills complete space
  - **Best thermal and mechanical reliability performance**



- **Partial Underfill or Edge Bond**
  - Dispensed “L” shape fillets along corners after reflow depending on bump array
  - Improvement in mechanical reliability (limited in thermal reliability)
  - No underfill in center for best RF transmission



CAPILLARY UNDERFILL BASICS

TYPICAL MATERIAL PROPERTIES

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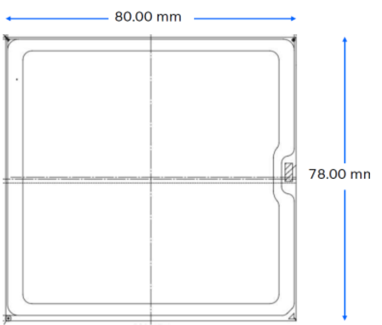
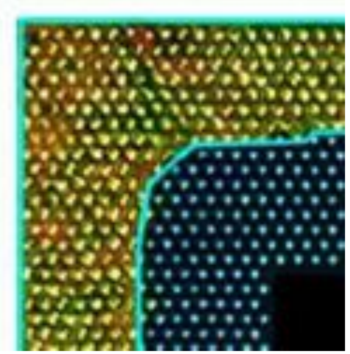
LOCTITE® ECCOBOND	Units	UF 8830S	UF 1173	UF 1175
Application	**-**	**Package Level**	**Board Level**	**Partial Underfill**
Color	-	Gray	Black	White
Filler Size	um	<5	<25	<20
Viscosity	cPs	22,000 @ 5rpm	7,500 @ 10/s	35,000 @ 5rpm
Thixotropy Index	-	0.85	0.71	1.05
Work Life @ 25°C	hours	>24	>48	>24
Shelf Life @ -40°C	months	>12	>6	>6 (-20°C)
Tg by TMA	°C	118	160	154
CTE1 / CTE2	ppm	25 / 100	26 / 103	19 / 68
Storage Modulus @ 25°C	MPa	11,500	6,000	14,000
Dielectric Constant @ 25GHz / 50GHz	-	3.5 / 3.5	3.2 / 3.2	NA
Dissipation Factor @ 25GHz / 50GHz	-	0.018 / 0.028	0.020 / 0.036	NA
Curing Condition		2hrs @150°C	5min @150°C	15min @ 120°C

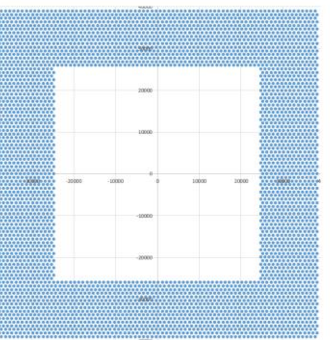
CAPILLARY UNDERFILL BASICS

EDGE FILL / PARTIAL UNDERFILL

- LOCTITE® ECCOBOND **UF 1175** – One component, low temperature cure and low stress partial underfill for **larger chip sizes**, combining good productivity (UPH) and reliability with easy jet dispensing and controlled flow
  - **15min 120°C cure** being compatible with low temperature solder interconnects
  - **>150°C Tg and <20ppm CTE** for lowest warpage and package/bump stress
  - Passing solder joint resistance test after 2000 temp cycles (-40/+100°C) with ~80x80mm FCBGA on FR4 test board
  - When applied by jetting, 50 to 60°C nozzle heating is recommended
  - For faster flow, board should be heated to 70 to 100ºC







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ADVANCED UNDERFILL SOLUTIONS

NEW CUF DEVELOPMENT FOCUS

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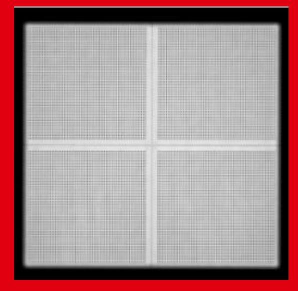
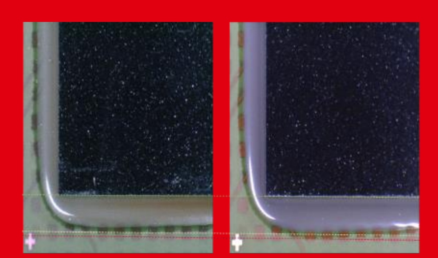
Larger die sizes



- Faster underfilling for high UPH
- Void-free underfill
- <5um fine filler cut for small gaps

More integration



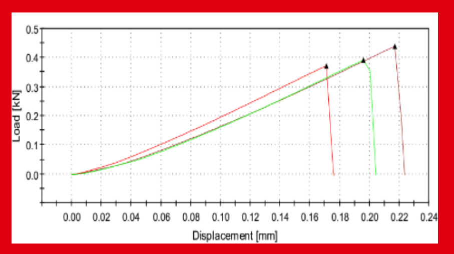
- Low resin bleed out (RBO) for tight Keep-out-Zone (KoZ)
- Improved adhesion to multiple interfaces
- Clean underfilling in varying fine gaps and pitches

Higher reliability

- Passing MSL3 and Temp Cycling (-55/125°C) on large Flip Chips

>1000TC on 30x30mm FC
>2000TC on 20x20mm FC

Narrow Si node



- Fracture toughness (K1c) enhancement for die crack reduction on smaller nodes
- Lower modulus, lower stress
- High Tg, ultra-low CTE

ADVANCED UNDERFILL SOLUTIONS

LOCTITE® ECCOBOND CUF EVOLUTION

UF 8830S	UF 8000AA	UF 8200HT	UF 9000AG	UF 9000AE
▪ Passing MSL L3/L2A and **consumer and AUTO reliability** on 10x10mm FC : - 5000TC (-55/125°C) - 4000TC (-55/150°C) ▪ Small filler size for narrow gaps	▪ Designed for **Chip-on-Wafer (CoW) application** ▪ Long staging time ▪ Fast flow for high output (UPH) ▪ Good reliability performance	▪ Designed for **higher thermal conductivity (1.2 W/mK)** ▪ Long staging time for Chip-on-Wafer ▪ Low CTE ▪ Good reliability performance	▪ Designed for **leading Si nodes** ▪ **30% faster flow for high UPH** ▪ Long staging time ▪ Low resin bleed out ▪ High Tg, lower CTE ▪ Good reliability performance	▪ Designed for larger **>20x20mm FC** ▪ Fast flow and long staging time ▪ Low shrinkage ▪ Higher toughness ▪ **Passing reliability on >110x110mm package designs**

ADVANCED UNDERFILL SOLUTIONS

RHEOLOGY FORMULATED FOR **LARGE DIE**

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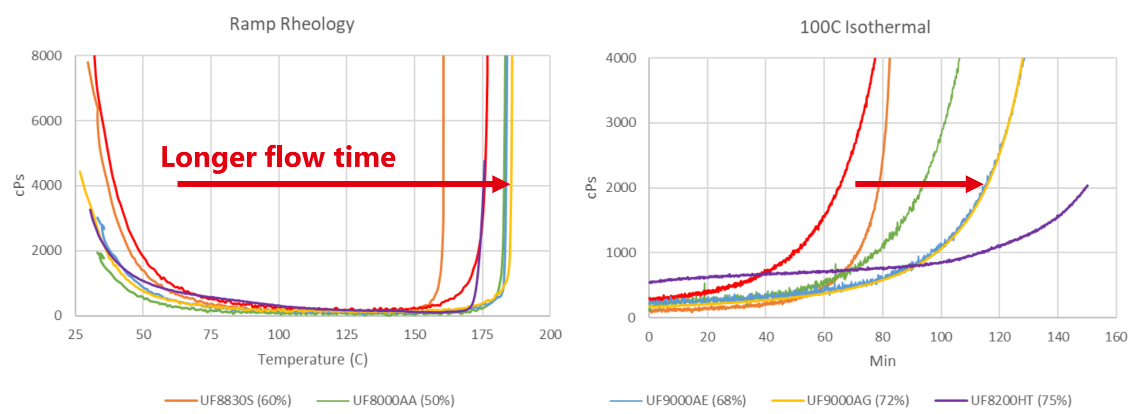
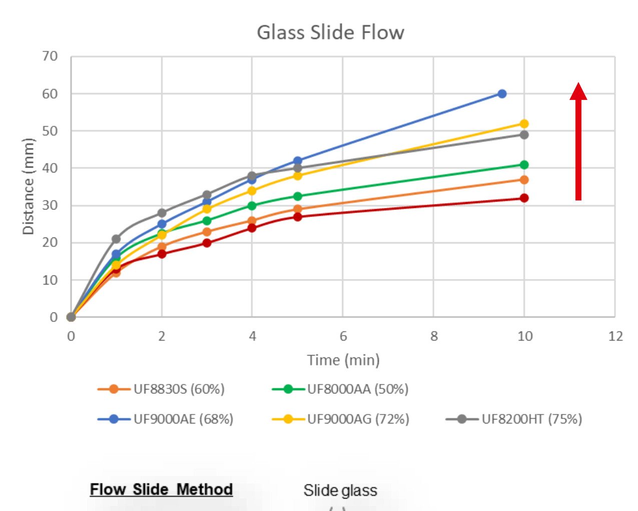
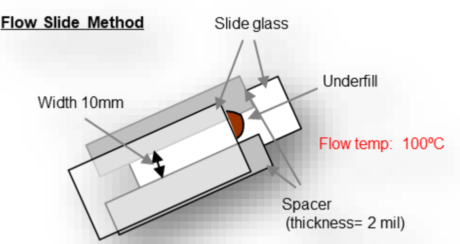


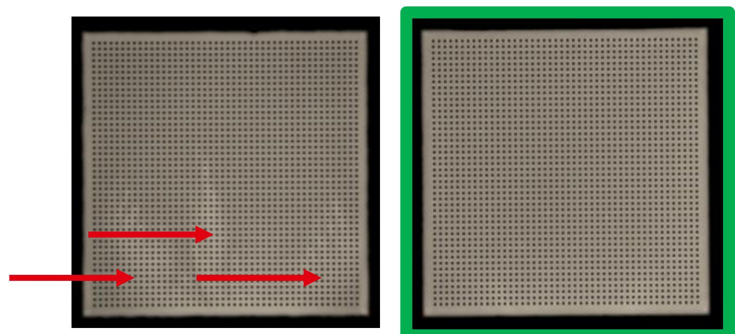


- **FAST flow**, >30% improvement compared to benchmark material
- Long **staging time** (>1 hour)
- Excellent **void-free gap filling** capability
- Highly filled formulations with selected fillers, resins and hardeners

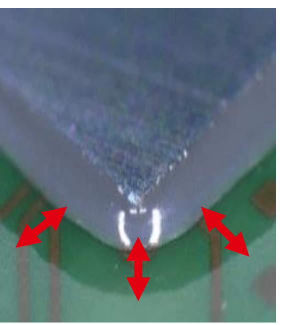


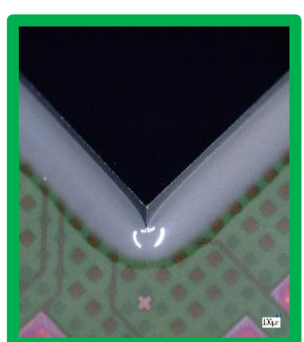
ADVANCED UNDERFILL SOLUTIONS

FORMULATED FOR **MORE INTEGRATION**



CSAM images with and without flow marks

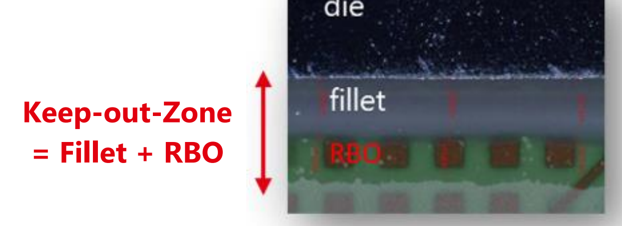




Optical images with high and low resin bleed out (RBO)

- **No flow marks** in thin gap applications
- Controlled and small fillet and minimal resin bleed out (RBO) for high integration (like multi-chip package with passives)
- Technical advantage derived from filler loading, filler size and combination of unique resins in CUF platform

Keep-out-Zone
= Fillet + RBO



ADVANCED UNDERFILL SOLUTIONS
FORMULATED FOR **HIGHER RELIABILITY**

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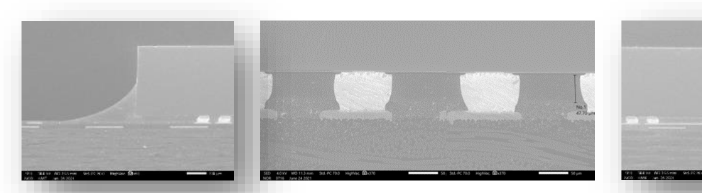
TV with 10x10mm die				
Underfill	**UF 8830S**	**UF 8000AA**	**UF 8200HT**	**UF 9000AG**
Filler loading	60%	50%	75%	72%
MSL2 / 3a	Pass / Pass	NA / Pass	NA / Pass	Pass / Pass
>1000 TC-B (-55C to 125°C)	Pass 5000	Pass 1000	Pass 1000	Pass 1000
>400 TC-C (-55C to 150°C)	Pass 4000	Not tested	Not tested	Pass 1400
HTS @ 150°C	Pass 1000h	Pass 1000h	Pass 1000h	Pass 1250h
uHAST (130°C, 85%RH)	Pass 264h	Pass 96h	Pass 96h	Pass 288h

TV with 20x20mm die		
Underfill	**UF 9000AG**	**UF 9000AE**
Filler loading	72%	**68%**
MSL3a	Pass	**Pass**
>1000 TC-B (-55C to 125°C)	Ongoing	**Pass 2000**
>400 TC-C (-55C to 150°C)	Pass 600	**Pass 600**
HTS @ 150°C	Pass 250h	**Pass 1000h**
uHAST (130°C, 85%RH)	Pass 96h	**Pass 192h**

- **UF 8830S and UF 9000AG passing Auto Grade 1** (UF 9000AG Grade 0 pending) by optimizing adhesion, Tg and modulus



ADVANCED UNDERFILL SOLUTIONS
FORMULATED FOR **NARROW SI NODE**

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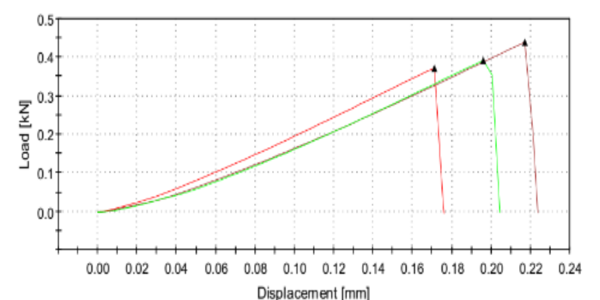
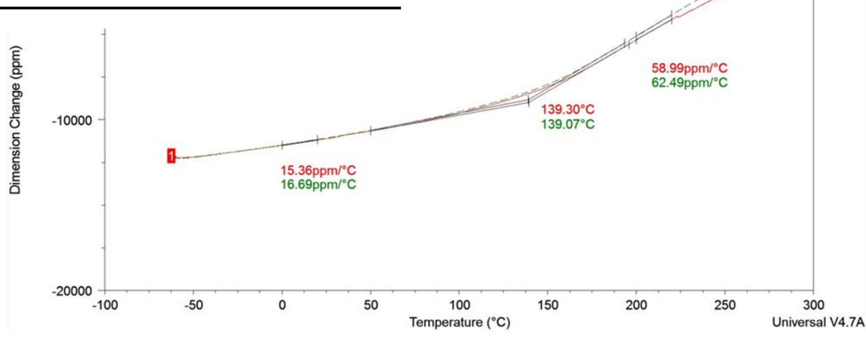
Fracture Toughness (K1c) and CTE improvement

Underfill	Unit	UF 8830S	UF 8000AA	UF 9000AG	UF 9000AE
Application	-	FC-CSP	FC-CSP, PoP	3-5nm node	Large die
Production	-	Volume	Volume	Volume	Scale-up
Filler loading	%	60	50	72	68
Filler size (avg)	um	0.5	0.5	1	1
Toughness (K1c)	MPa√m	2.0	0.6	**3.0**	**2.9**
CTE1 / CTE2	ppm/°C	25 / 100	30 / 119	**19 / 62**	23 / 84

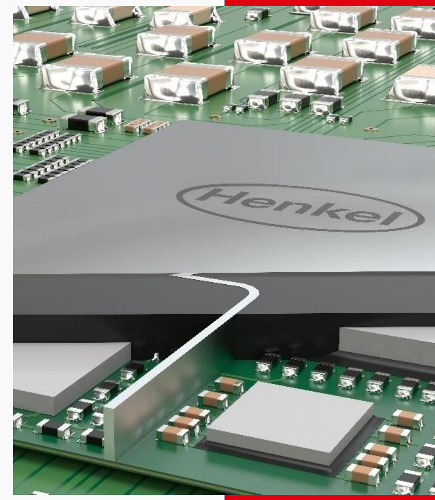


- **Higher fracture toughness (K1c) and lower CTE** enabling leading edge **3nm and 5nm Si nodes**
- Technical advantage derived from higher filler loading, filler size and tougher resin systems



KEY TAKEAWAYS

- Heterogeneous Integration and advanced flip-chip architectures are essential elements for many end applications in automotive, high-performance computing, mobile and consumer electronics
- New package architectures continue to face ‘stressful packaging’ challenges to address reliability and performance
- Addressing these challenges require innovation in semiconductor packaging materials and processes (to extend ‘Moore’s Law’)
- Henkel’s new developments in low warpage liquid encapsulants and advanced capillary underfills are well positioned and recognized to solve these challenges



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Many Thanks !

Ruud de Wit |
Henkel Electronic Materials

Business Development | Semiconductor, Sensor and Consumer Electronics Assembly Solutions

+31 643 372 108 | ruud.dewit@henkel.com
www.henkel-adhesives.com/electronics